REMARKS

In the Office Action dated September 30, 2003, claims 1-28 are noted as pending. Claims 25-28 are rejected under 35 USC 102(e) as being anticipated by Kumar et al., U.S. Patent No. 6,247,094 (hereinafter Kumar). Claims 1-18 are rejected as being unpatentable over Saulsbury et al., U.S. Patent No. 6,128,702 (hereinafter Saulsbury) in view of Kumar. Claims 19-24 are rejected under 35 USC 103(a) as being unpatentable over Westberg et al., U.S. Patent No. 5,361,391 (hereinafter Westberg) in view of Saulsbury and in further view of Kumar.

Objections to the Specification

The specification has been amended to cure the informality.

REJECTIONS UNDER 35 U.S.C. 102(e)

Kumar does not disclose "delivering during a first plurality of transfer periods information corresponding to both an activate command and a cache fetch command from a memory controller to a memory module over a memory bus; and

delivering from the memory controller to the memory module during a last transfer period information differentiating between an activate command and a cache fetch command" as claimed in claim 25 (emphasis added).

Further, Kumar does not disclose "delivering during a first plurality of transfer periods information corresponding to both a read command and a read and preload command from a memory controller to a memory module over a memory bus; and

delivering from the memory controller to the memory module during a last transfer period information differentiating between a read command and a read and preload command" as claimed in claim 27 (emphasis added).

For these reasons, claims 25-28 are not anticipated by Kumar.

REJECTIONS UNDER 35 U.S.C. 103(a)

Neither Saulsbury, nor Kumar, nor Westberg, either alone or in combination, disclose a data cache located on a memory module controlled by a command sequencer and serializer unit in a memory controller where the memory controller and memory module are coupled together via a memory bus as claimed in amended claim 1. It should be noted that the command sequence and serializer unit and array of tag addresses are not located on the memory module, as indicated by the language of claim one describing a memory bus coupling the memory controller the memory module.

Claims 13 and 17 similarly include limitations where the array of tags are located in a memory controller and the data cache is located on a memory module.

For these reasons, claims 1-24 are patentable over the Saulsbury, Kumar, and Westberg references.

CONCLUSION:

In view of the foregoing, Applicant submits that claims 1-28 are distinguished over the cited art and are in condition for allowance. Allowance of claims 1-28 is respectfully requested.

DEPOSIT ACCOUNT AUTHORIZATION

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any additional charges that may be due.

Respectfully submitted,

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